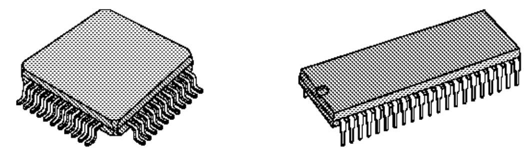
SGS-THOMSON MICROELECTRONICS

TDA7344

DIGITAL CONTROLLED AUDIO PROCESSOR WITH SURROUND SOUND MATRIX

PRODUCT PREVIEW

- 1 STEREO INPUT
- VOLUME CONTROL IN 1.25dB STEP
- TREBLE AND BASS CONTROL
- THREE SURROUND MODES ARE AVAILABLE:
  – MOVIE, MUSIC AND SIMULATED
- FOUR SPEAKER ATTENUATORS:
  – 4 INDEPENDENT SPEAKERS CONTROL IN 1.25dB STEPS FOR BALANCE FACILITY
  – INDEPENDENT MUTE FUNCTION
- ALL FUNCTIONS PROGRAMMABLE VIA SERIAL BUS



PQFP44 (10 X 10) **SDIP42**

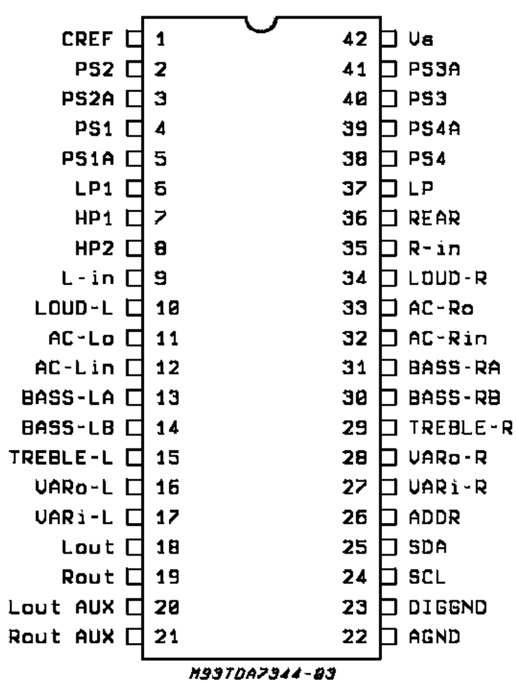
ORDERING NUMBER: TDA7344P (PQFP44)
TDA7344S (SDIP42)

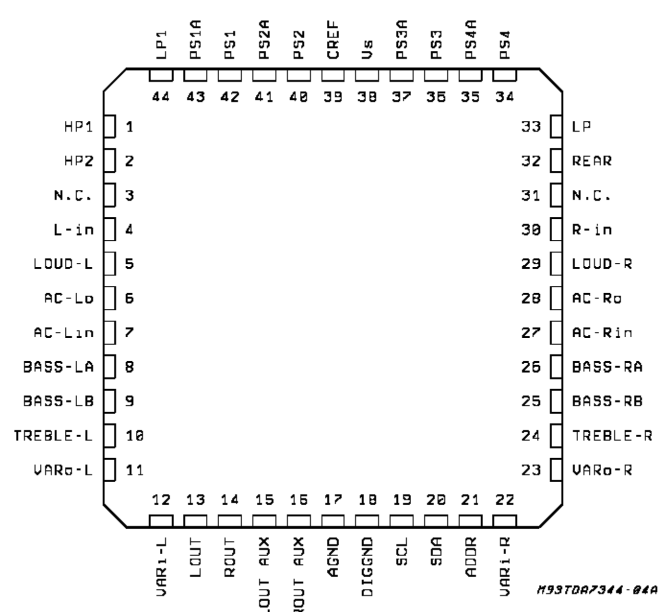
DESCRIPTION

The TDA7344 is a volume tone (bass and treble) balance (Left/Right) processor for quality audio applications in car radio and Hi-Fi systems.
It reproduces surround sound by using phase shifters and a signal matrix. Control of all the functions is accomplished by serial bus.
The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

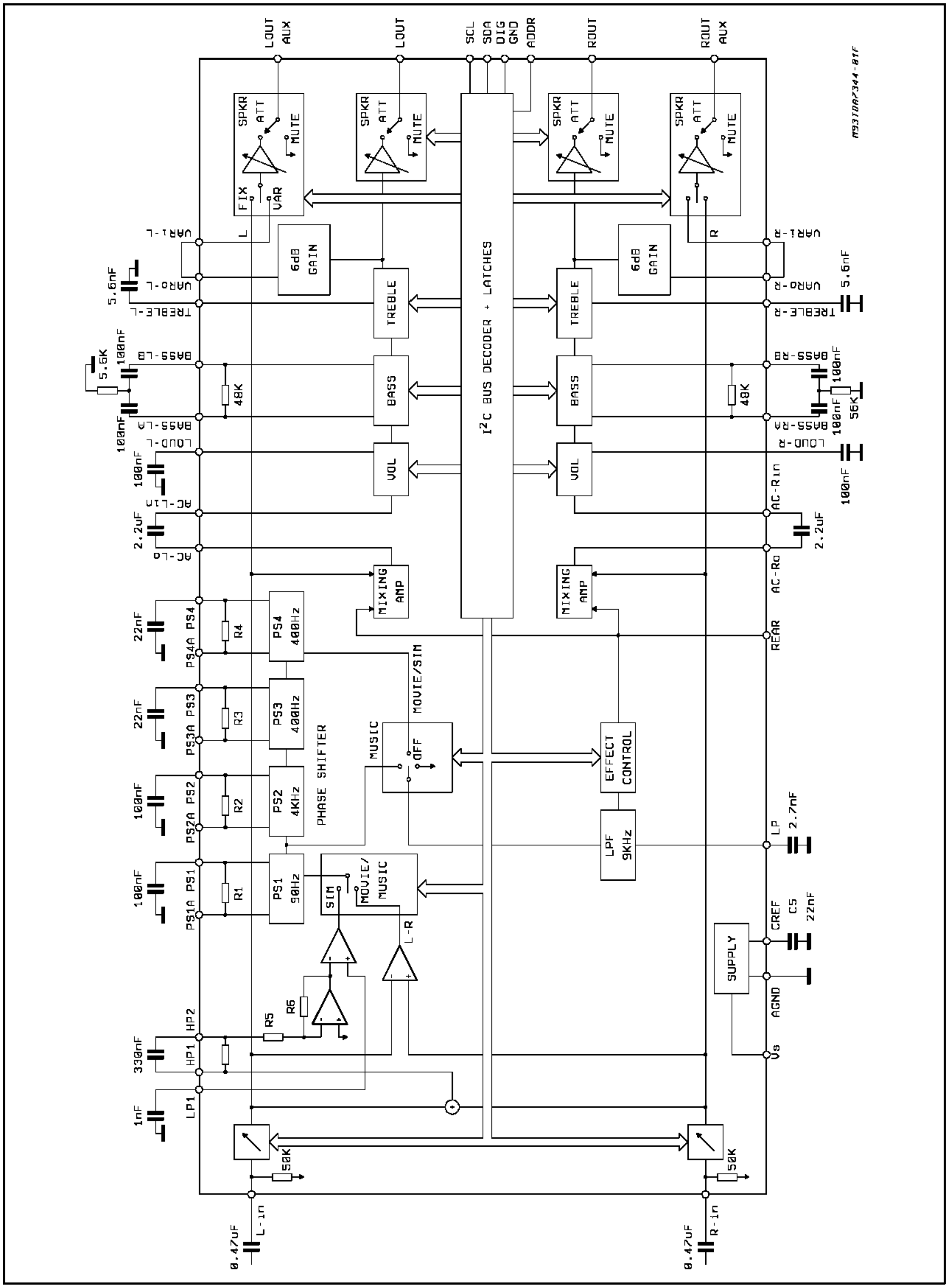
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained.

PIN CONNECTION

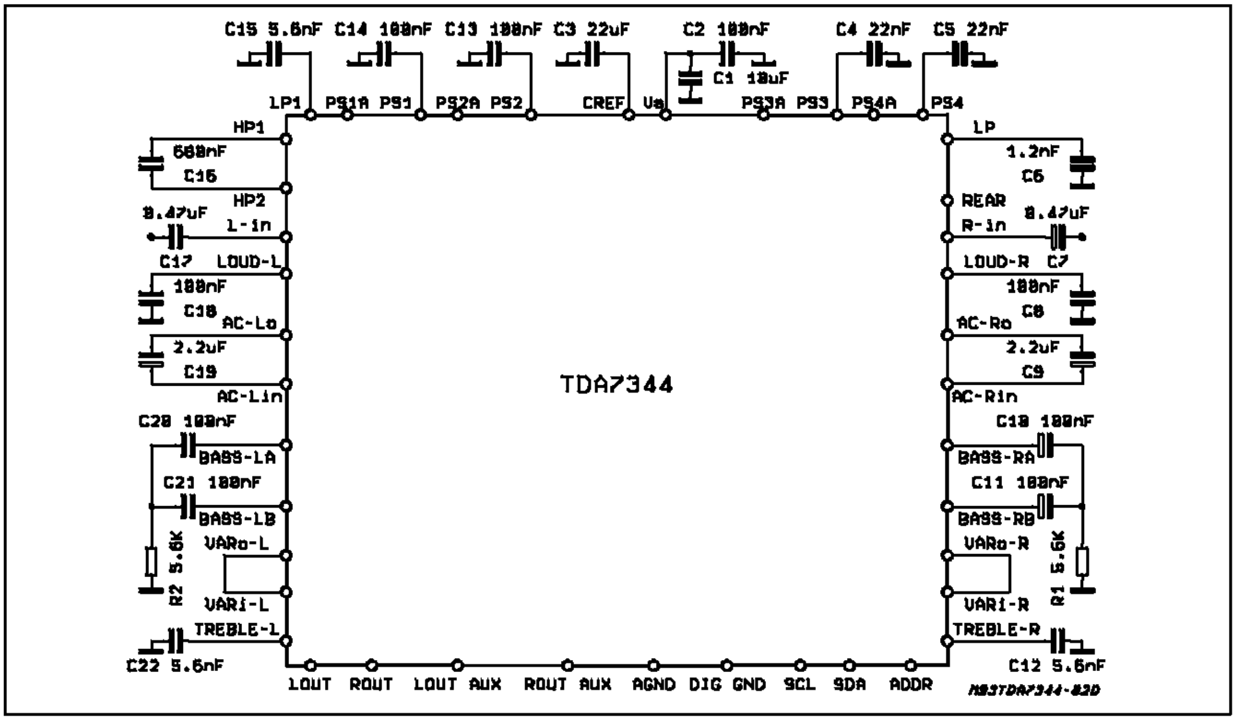




BLOCK DIAGRAM



TEST CIRCUIT



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	85	°C/W

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	11	V
T_{amb}	Operating Ambient Temperature	-10 to 85	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

QUICK REFERENCE DATA

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_S	Supply Voltage	7	9	10.5	V
V_{CL}	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion V = 1Vrms f = 1KHz		0.02	0.1	%
S/N	Signal to Noise Ratio V_{out} = 1Vrms (made = OFF)		106		dB
S_C	Channel Separation f = 1KHz		70		dB
	Volume Control 1.25dB step	-78.75		0	dB
	Treble Control (2db step)	-14		+14	dB
	Bass Control (2db step)	-14		+14	dB
	Balance Control 1.25dB step (L_{CH}, R_{CH})	-38.75		0	dB
	Mute Attenuation		90		dB

ELECTRICAL CHARACTERISTICS (refer to the test circuit T_{amb} = 25°C, V_S = 9V, R_L = 10KΩ, R_G = 600Ω, all controls flat (G = 0),Effect Ctrl = -6dB, MODE = OFF; f = 1KHz unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_S	Supply Voltage		7	9	10.5	V
I_S	Supply Current			25		mA
SVR	Ripple Rejection	L_{CH} / $R_{CH\ out}$, Mode = OFF	60	80		dB
INPUT STAGE						
R_{II}	Input Resistance			50		KΩ
V_{CL}	Clipping Level	THD = 0.3%; Lin or Rin	2	2.5		Vrms
		THD = 0.3%; Rin + Lin (2)		3.0		Vrms
C_{RANGE}	Control Range			20		dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation			20		dB
A_{STEP}	Step Resolution			0.31		dB
V_{DC}	DC Steps	adjacent att. step		0		mV
VOLUME CONTROL						
C_{RANGE}	Control Range		70	75	80	dB
A_{VMIN}	Min. Attenuation		-1	0	1	dB
A_{VMAX}	Max. Attenuation		70	75	80	dB
A_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation Set Error	Av = 0 to -20dB Av = -20 to -60dB	-1.5 -3	0	1.5 2	dB dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	adjacent attenuation steps From 0dB to Av max		0 0.5		mV mV
BASS CONTROL (1)						
Gb	Control Range	Max. Boost/cut	±12	±14	±16	dB
B_{STEP}	Step Resolution		1	2	3	dB
R_B	Internal Feedback Resistance		32	44	56	KΩ
TREBLE CONTROL (1)						
Gt	Control Range	Max. Boost/cut	±13	±14	±15	dB
T_{STEP}	Step Resolution		1	2	3	dB
EFFECT CONTROL						
C_{RANGE}	Control Range		- 21		- 6	dB
S_{STEP}	Step Resolution			1		dB

ELECTRICAL CHARACTERISTICS (continued)

SURROUND SOUND MATRIX

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{OFF}	In-phase Gain (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p}, $R_{in} \rightarrow R_{out}$ $L_{in} \rightarrow L_{out}$	-1.5	0	1.5	dB
D_{GOFF}	LR In-phase Gain Difference (OFF)	Mode OFF, Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$), ($L_{in} \rightarrow L_{out}$)	-1.5	0	1.5	dB
G_{MOV1}	In-phase Gain (Movie 1)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$		7		dB
G_{MOV2}	In-phase Gain (Movie 2)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$		8		dB
D_{GMOV}	LR In-phase Gain Diffrence (Movie)	Movie mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$) – ($L_{in} \rightarrow L_{out}$)		0		dB
G_{MUS1}	In-phase Gain (Music 1)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$) – ($L_{in} \rightarrow L_{out}$)		6		dB
G_{MUS2}	In-phase Gain (Music 2)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} $R_{in} \rightarrow R_{out}$, $L_{in} \rightarrow L_{out}$		7.5		dB
D_{GMUS}	LR In-phase Gain Difference (Music)	Music mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p} ($R_{in} \rightarrow R_{out}$) – ($L_{in} \rightarrow L_{out}$)		0		dB
L_{MON1}	Simulated L Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		4.5		dB
L_{MON2}	Simulated L Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		– 4.0		dB
L_{MON3}	Simulated L Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow L_{out}$		7.0		dB
R_{MON1}	Simulated R Output 1	Simulated Mode, Effect Ctrl = -6dB Input signal of 250Hz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		– 4.5		dB
R_{MON2}	Simulated R Output 2	Simulated Mode, Effect Ctrl = -6dB Input signal of 1kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		3.8		dB
R_{MON3}	Simulated R Output 3	Simulated Mode, Effect Ctrl = -6dB Input signal of 3.6kHz, 1.4 V_{p-p}, R_{in} and $L_{in} \rightarrow R_{out}$		– 20		dB
R_{LP1}	Low Pass Filter Resistance			10		KΩ
R_{PS1}	Phase Shifter 1 Resistance			17.95		kΩ
R_{PS2}	Phase Shifter 2 Resistance			0.398		KΩ
R_{PS3}	Phase Shifter 3 Resistance			18.08		KΩ
R_{PS2}	Phase Shifter 4 Resistance			18.08		KΩ
R_{HPI}	High Pass Filter Resistance			60		KΩ
R_{LPF}	LP Pin Impedance			10		KΩ

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SPEAKER ATTENUATORS						
C_{range}	Control Range		35	37.5	40	dB
S_{STEP}	Step Resolution		0.5	1.25	1.75	dB
E_A	Attenuation set error		-1.5		1.5	dB
A_{MUTE}	Output Mute Attenuation			90		dB
V_{DC}	DC Steps	adjacent att. steps from 0 to mute		0 1		mV mV
SPEAKER ATTENUATORS AUX						
C_{range}	Control Range		70	75	80	dB
S_{STEP}	Step Resolution			1.25		dB
E_A	Attenuation set error	Av = 0 to 20dB	-1.5	0	1.5	dB
		Av = -20 to -60dB	-3	0	2	dB
V_{DC}	DC Steps	adjacent att. steps		0	3	mV
A_{MUTE}	Output Mute Attenuation			90		dB
AUDIO OUTPUTS						
V_{OCL}	Clipping Level	d = 0.3%	2	2.5		Vrms
R_{OUT}	Output resistance		100	200	300	Ω
V_{OUT}	DC Voltage Level		4.2	4.5	4.8	V
GENERAL						
$N_{O(OFF)}$	Output Noise (OFF)	Output Muted, B_W = 20Hz to 20KHz R_{out} and I_{out} measurement		4 8		µVrms µVrms
$N_{O(MOV)}$	Output Noise (Movie)	Mode =Movie , B_W = 20Hz to 20KHz R_{out} and L_{out} measurement		30		µVrms
$N_{O(MUS)}$	Output Noise (Music)	Mode = Music , B_W = 20Hz to 20KHz, R_{out} and L_{out} measurement		30		µVrms
$N_{O(MON)}$	Output Noise (Simulated)	Mode = Simulated, B_W = 20Hz to 20KHz R_{out} and L_{out} measurement		30		µVrms
d	Distorsion	Av = 0 ; V_{in} = 1Vrms		0.02	0.1	%
S_C	Channel Separation			70		dB
BUS INPUTS						
V_{IL}	Input Low Voltage				1	V
V_{IH}	Input High Voltage		3			V
I_{IN}	Input Current		-5		+5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Note:

(1) Bass and Treble response: The center frequency and the resonance quality can be choosen by the external circuitry. A standard first order bass response can be realized by a standard feedback network.

(2) The peack voltage of the two input signals must be less then $\frac{V_S}{2}$:

$$(Lin + Rin)_{peak} \bullet A_{Vin} < \frac{V_S}{2}$$

I^2C BUS INTERFACE

Data transmission from microprocessor to the TDA7344 and viceversa takes place through the 2 wires I^2C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

Data Validity

As shown in fig. 3, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop Conditions

As shown in fig.4 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 5). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

The audioprocessor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

Transmission without Acknowledge

Avoiding to detect the acknowledge of the audioprocessor, the µP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data.

This approach of course is less protected from misworking and decreases the noise immunity.

Figure 3: Data Validity on the I^2CBUS

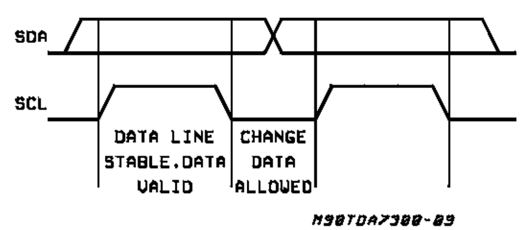


Figure 4: Timing Diagram of I^2CBUS

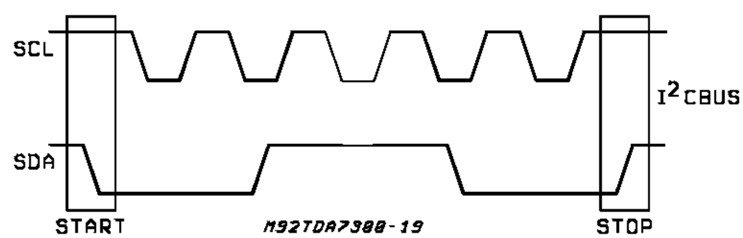
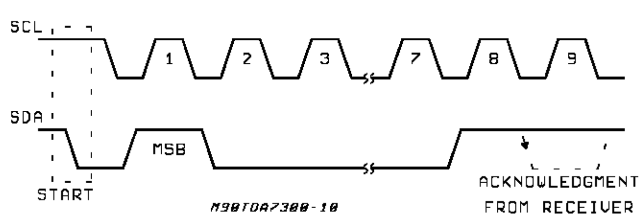


Figure 5: Acknowledge on the I^2CBUS

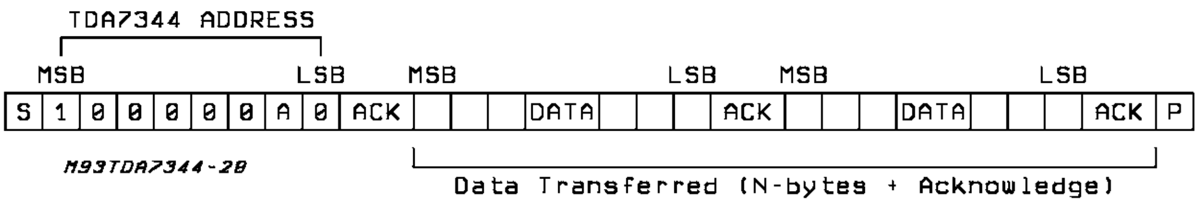


SOFTWARE SPECIFICATION

Interface Protocol

The interface protocol comprises:

- A start condition (s)
- A chip address byte, containing the TDA7344 address (the 8th bit of the byte must be 0). The TDA7344 must always acknowledge at the end of each transmitted byte.
- A subaddress (function) bytes (identified by the MSB = 0)
- A sequence of dates and subaddresses (N bytes + achnowledge. The dates are identified by MSB = 1, subaddresses by MSB = 0)
- A stop condition (P)



ACK = Achnowledge
S = Start
P = Stop

INTERFACE FEATURES

- Due to the fact that the MSB is used to select if the byte transmitted is a subaddress (function) or a data (value), between a start and stop condition, is possible to receive, how many subaddresses and datas as wanted.
- The subaddress (function) is fixed until a new subaddress is transmitted, so the TDA7344 can receive how many data as wanted for the selected subaddress (without the need for a new start condition)
- If TDA7344 receives a subaddress with the LSB = 1 the incremental bus is selected, so it enters in a loop condition that means that every acknowledge will increase automatically the subaddress (function) and it receives the data related to the new subaddress.

So it can receive in a single transmission how many subaddress are necessary, and for each subaddress how many data are necessary.

EXAMPLES

1) NO INCREMENTAL BUS

TDA7344 receives a start condition, the correct chip address, a subaddress with the LSB = 0 (no incremental bus), N-datas (all these datas concern the subaddress selected), a new subaddress, N-data, a stop condition.

2) INCREMENTAL BUS

TDA7344 receives a start condition, the correct chip address a subaddress with the LSB = 1 (incremental bus): now it is in a loop condition with an autoincrease of the subaddress.
The first data that it receives doesn't concern the subaddress sended but the next one, the second one concerns the subaddress sended plus two in the loop etc, and at the end it receives the stop condition.

In the pictures there are some examples:

S = start

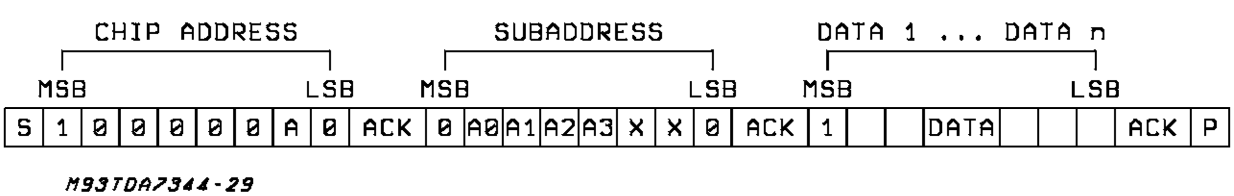
A	CHIP ADDRESS
0	80 (HEX)
1	82 (HEX)

ACK = acknowledge

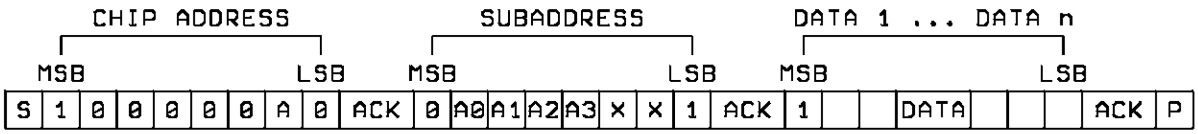
B = 1 incremental bus, B = 0 no incremental bus

P = stop

1) one subaddress, with n data concerning that subaddress (no incremental bus)

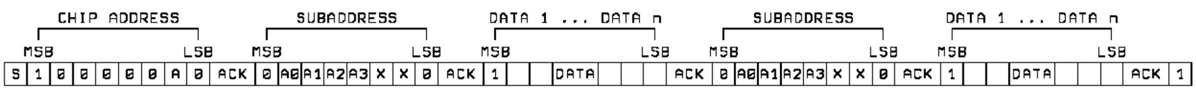


2) one subaddress, (with incremental bus) , with n data (data1 that concerns subaddress +1, data 2 that concerns subaddress + 2 etc.)



M93TDA7344-30

3) more subaddress with more data



M93TDA7344-31

DATA BYTES

FUNCTION SELECTION
FIRST BYTE (subaddress)

The first byte select the function, it is identified by the MSB = 0

MSB							LSB	SUBADDRESS
	A0	A1	A2	A3			B	
0	0	0	0	X	X	X	B	VOLUME ATTENUATION & LOUDNESS
0	1	0	0	X	X	X	B	SURROUND & OUT & EFFECT CONTROL
0	0	1	0	X	X	X	B	BASS
0	1	1	0	X	X	X	B	TREBLE
0	0	0	1	X	X	X	B	ATT SPEAKER R
0	1	0	1	X	X	X	B	ATT SPEAKER L
0	0	1	1	X	X	X	B	ATT. ROUT AUX
0	1	1	1	0	X	X	B	ATT. LOUT AUX
0	1	1	1	1	X	X	B	INPUT STAGE CONTROL

B = 1 yes incremental bus;
B = 0 no incremental bus;
X = indifferent 0,1

VALUE SELECTION

The second byte select the value, it is identified by the MSB = 1

VOLUME ATTENUATION								
MSB							**LSB**	**1.25 dB STEPS**
1					0	0	0	0
1					0	0	1	-1.25
1					0	1	0	-2.50
1					0	1	1	-3.75
1					1	0	0	-5.00
1					1	0	1	-6.25
1					1	1	0	-7.50
1					1	1	1	-8.75
								10 dB STEPS
1		0	0	0				0
1		0	0	1				-10
1		0	1	0				-20
1		0	1	1				-30
1		1	0	0				-40
1		1	0	1				-50
1		1	1	0				-60
1		1	1	1				-70
SELECTION								**LOUDNESS**
1	0							ON
1	1							OFF

ATT AUX OUT1 AND 2								
MSB							**LSB**	**1.25 dB STEPS**
1					0	0	0	0
1					0	0	1	-1.25
1					0	1	0	-2.50
1					0	1	1	-3.75
1					1	0	0	-5.00
1					1	0	1	-6.25
1					1	1	0	-7.50
1					1	1	1	-8.75
								10 dB STEPS
1		0	0	0				0
1		0	0	1				-10
1		0	1	0				-20
1		0	1	1				-30
1		1	0	0				-40
1		1	0	1				-50
1		1	1	0				-60
1		1	1	1				-70
								MUTE
1	0							OFF
1	1							ON

ATT SPEAKER R AND L								
MSB							**LSB**	**1.25 dB STEPS**
1	X	X			0	0	0	0
1	X	X			0	0	1	-1.25
1	X	X			0	1	0	-2.50
1	X	X			0	1	1	-3.75
1	X	X			1	0	0	-5.00
1	X	X			1	0	1	-6.25
1	X	X			1	1	0	-7.50
1	X	X			1	1	1	-8.75
								10 dB STEPS
1	X	X	0	0				0
1	X	X	0	1				-10
1	X	X	1	0				-20
1	X	X	1	1				-30
1	X	X	1	1	1	1	1	MUTE

TREBLE/ BASS								
MSB							**LSB**	**2 dB STEPS**
1	X	X	X	0	1	1	1	14
1	X	X	X	0	1	1	0	12
1	X	X	X	0	1	0	1	10
1	X	X	X	0	1	0	0	8
1	X	X	X	0	0	1	1	6
1	X	X	X	0	0	1	0	4
1	X	X	X	0	0	0	1	2
1	X	X	X	0	0	0	0	0
1	X	X	X	1	0	0	0	0
1	X	X	X	1	0	0	1	-2
1	X	X	X	1	0	1	0	-4
1	X	X	X	1	0	1	1	-6
1	X	X	X	1	1	0	0	-8
1	X	X	X	1	1	0	1	-10
1	X	X	X	1	1	1	0	-12
1	X	X	X	1	1	1	1	-14

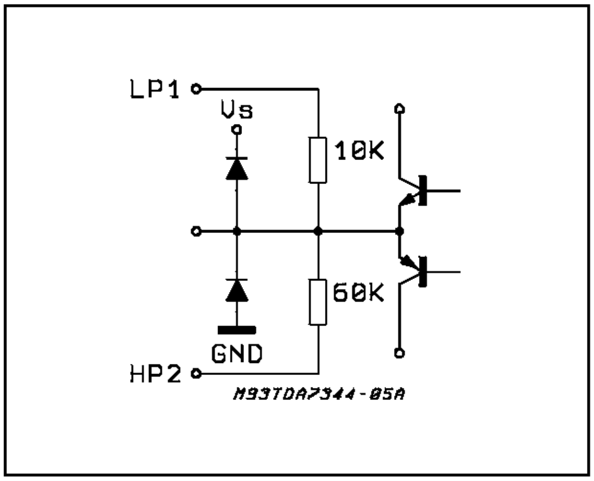
SURROUND & OUT & EFFECT CONTROL								
MSB							LSB	SELECTION
SELECTION								SURROUND
1						0	0	SIMULATED
1						0	1	MUSIC
1						1	0	MOVIE
1						1	1	OFF
SELECTION								OUT
1					0			OUT VAR
1					1			OUT FIX
SELECTION								EFFECT CONTROL
1	0	0	0	0				-6
1	0	0	0	1				-7
1	0	0	1	0				-8
1	0	0	1	1				-9
1	0	1	0	0				-10
1	0	1	0	1				-11
1	0	1	1	0				-12
1	0	1	1	1				-13
1	1	0	0	0				-14
1	1	0	0	1				-15
1	1	0	1	0				-16
1	1	0	1	1				-17
1	1	1	0	0				-18
1	1	1	0	1				-19
1	1	1	1	0				-20
1	1	1	1	1				-21

For example to select the music mode, out fix, effect control =-9dB:
1 0 0 1 1 1 0 1

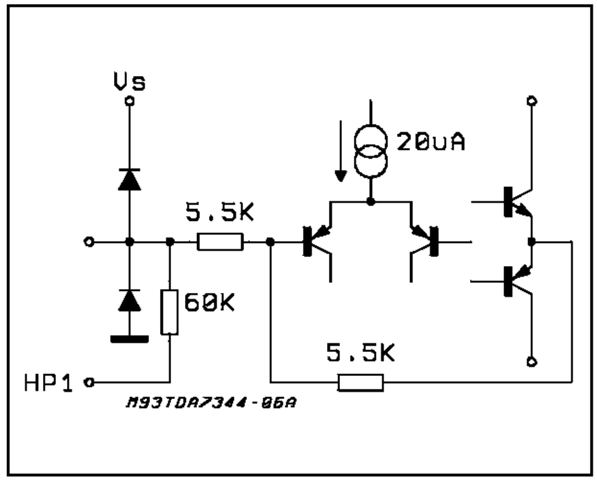
INPUT CONTROL RANGE (0 TO -19.68dB)								
MSB							**LSB**	**0.3125 dB STEPS**
1	X				0	0	0	0
1	Xx				0	0	1	-0.3125
1	X				0	1	0	-0.625
1	X				0	1	1	-0.9375
1	X				1	0	0	-1.25
1	X				1	0	1	-1.5625
1	X				1	1	0	-1.875
1	X				1	1	1	-2.1875
								2.5 dB STEPS
1	X	0	0	0				0
1	X	0	0	1				-2.5
1	X	0	1	0				-5.0
1	X	0	1	1				-7.5
1	X	1	0	0				-10
1	X	1	0	1				-12.5
1	X	1	1	0				-15
1	X	1	1	1				-17.5

POWER ON RESET	
VOLUME ATTENUATION	MAX ATTENUATION, LOUDNESS OFF
TREBLE	-14dB
BASS	-14dB
SURROUND & OUT CONTROL + EFFECT CONTROL	OFF + FIX + MAX ATTENUATION
ATT SPEAKER R	MUTE
ATT SPEAKER L	MUTE
ATT AUX OUT 1	MUTE
ATT AUX OUT 2	MUTE

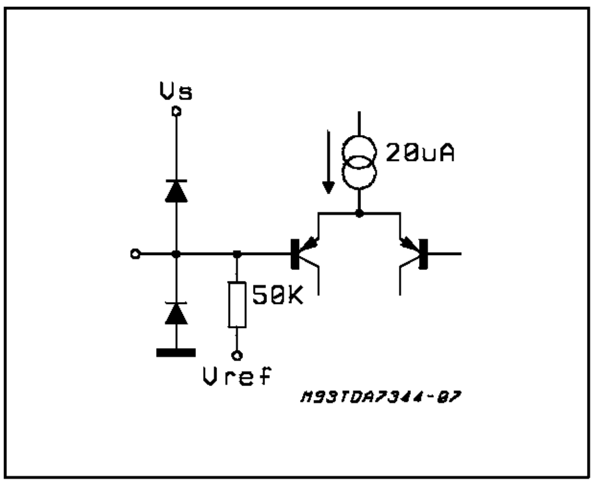
PIN: HP1



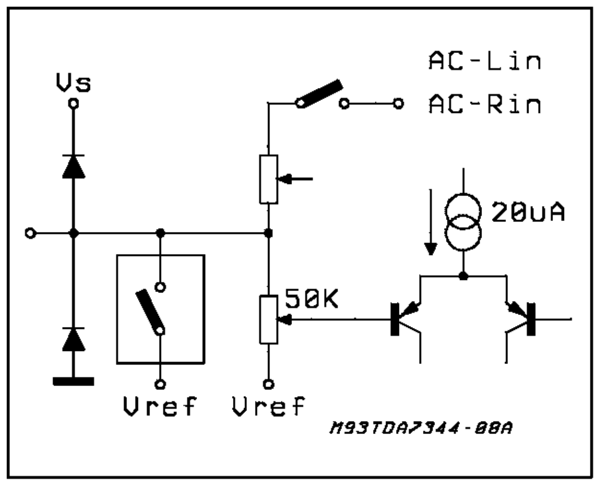
PIN: HP2



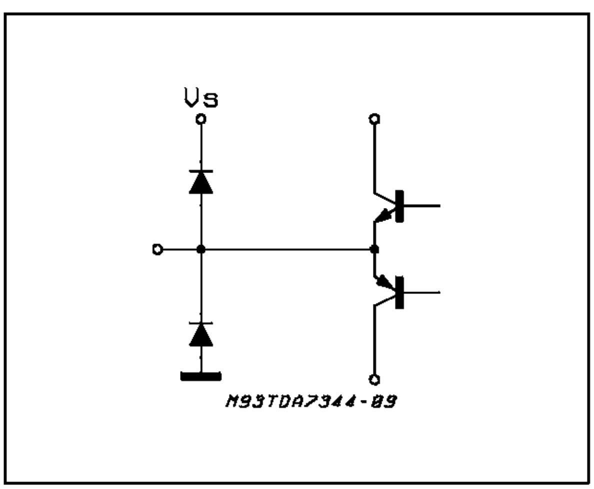
PIN: L_{in}, R_{in}



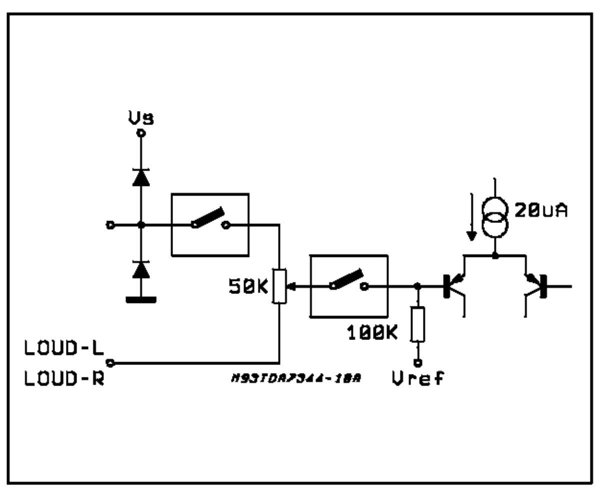
PIN: L_{OUD-R}, L_{OUB-L}



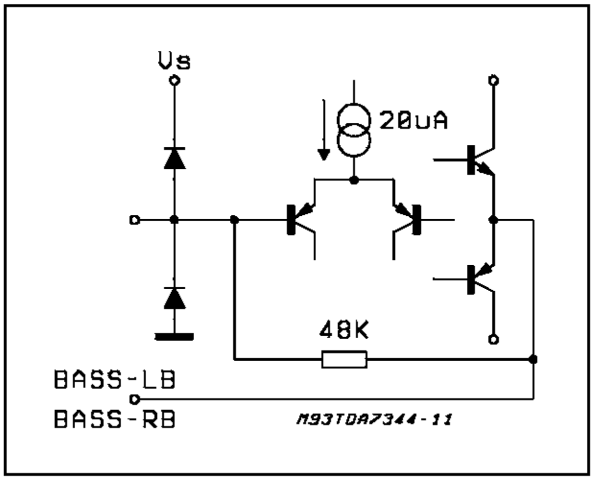
PIN: AC - L_O, AC - R_O,



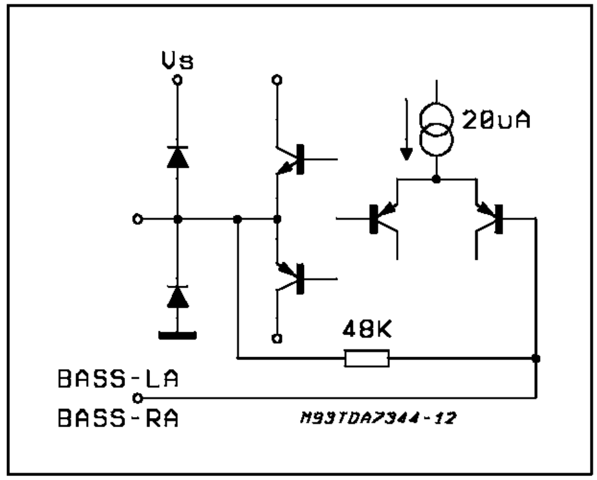
PIN: AC - L_{IN}, AC - R_{IN},



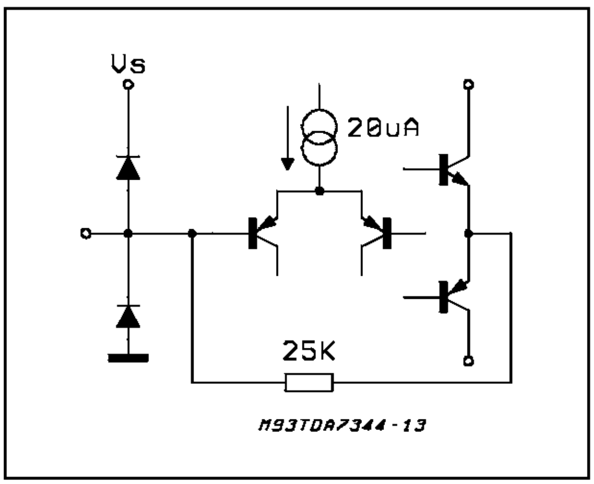
PIN: BASS - LA, BASS - RA



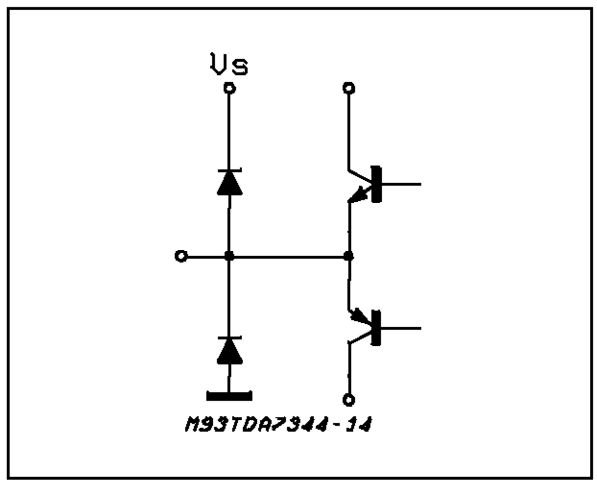
PIN: BASS - LB, BASS - RB



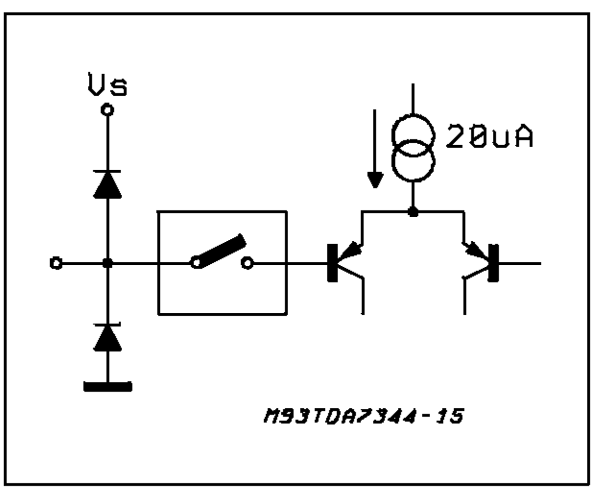
PIN: TREBLE - L, TREBLE - R



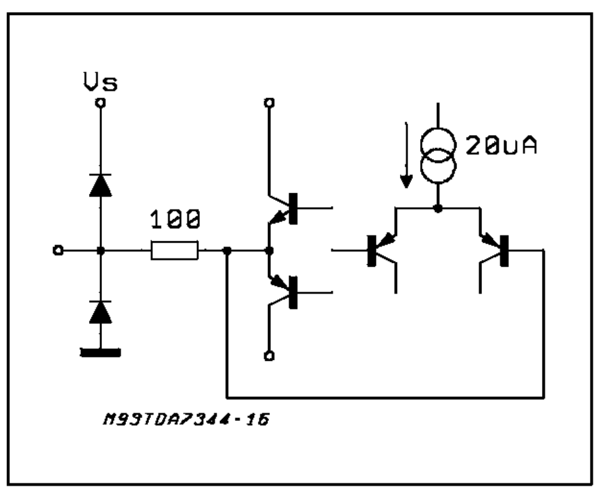
PIN: VAR_O **-** L, VAR_O -R



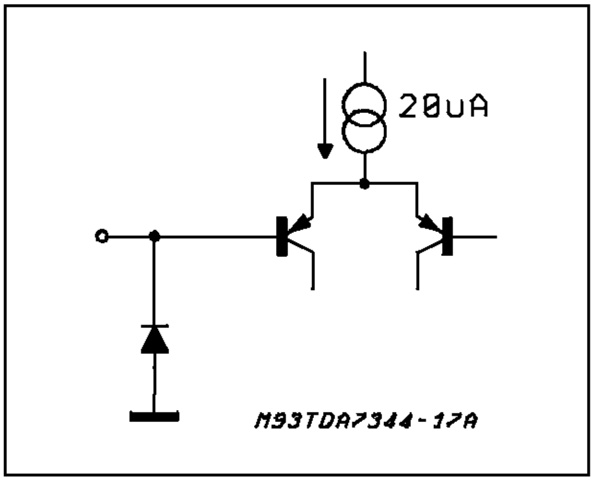
PIN: VAR_i **-** L, VAR_i -R



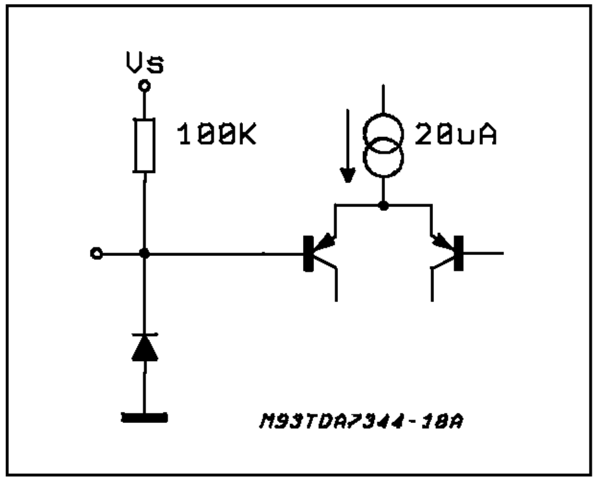
PIN: L_{OUT}, R_{OUT}, $L_{OUT\ AUX}$, $R_{OUT\ AUX}$, REAR



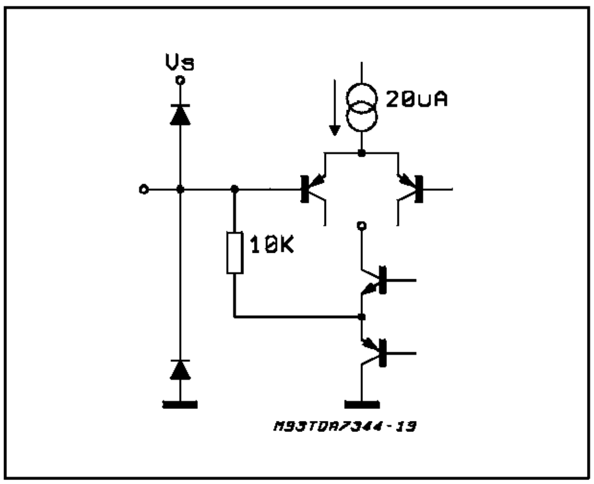
PIN: SCL, SDA



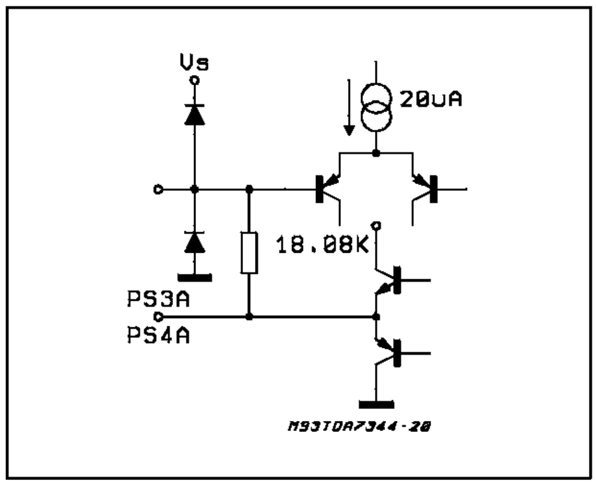
PIN: ADDR



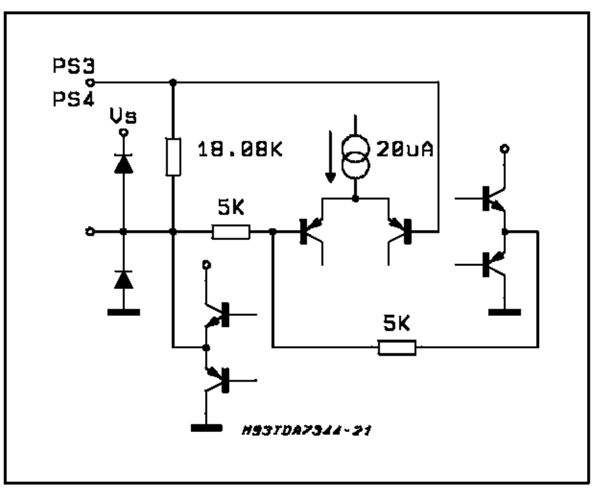
PIN: LP



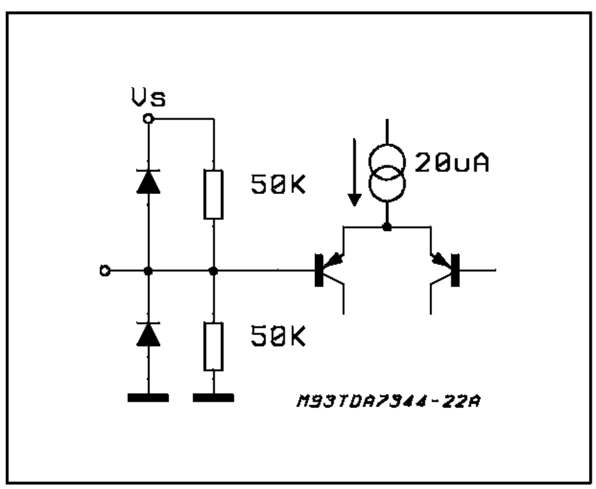
PIN: PS3, PS2



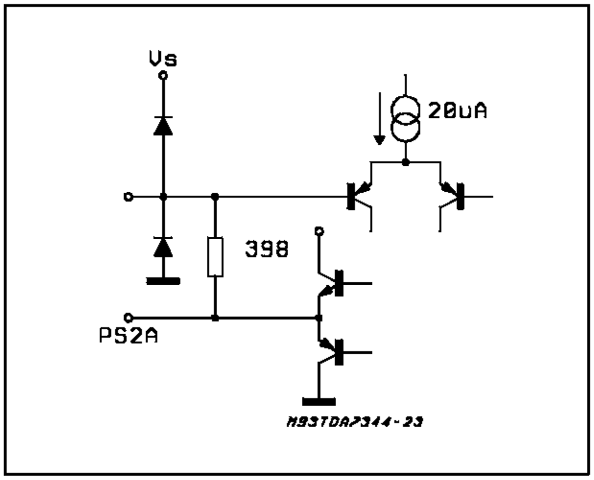
PIN: PS3A, PS4A



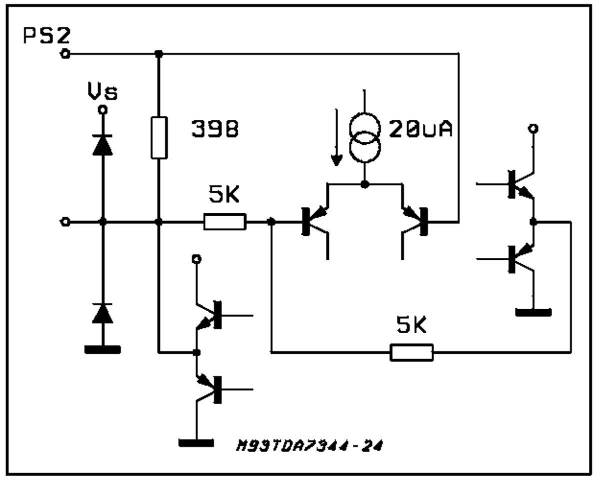
PIN: CREF



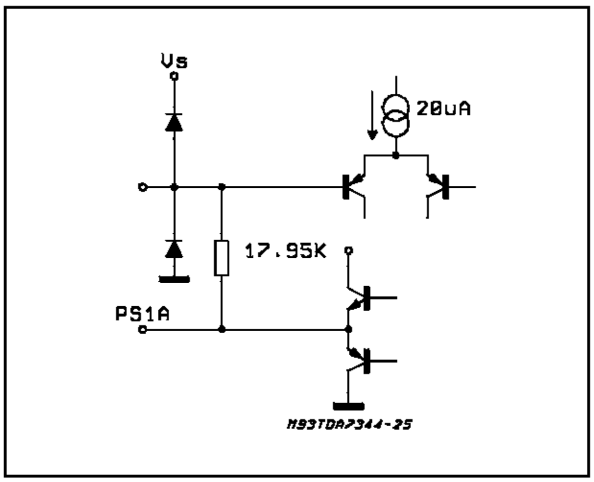
PIN: PS2



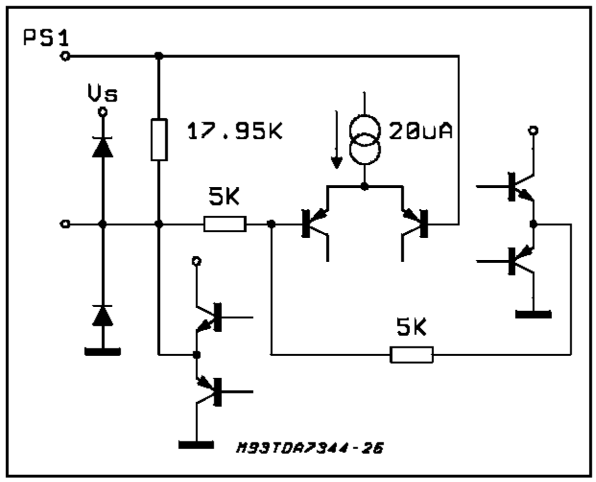
PIN: PS2A



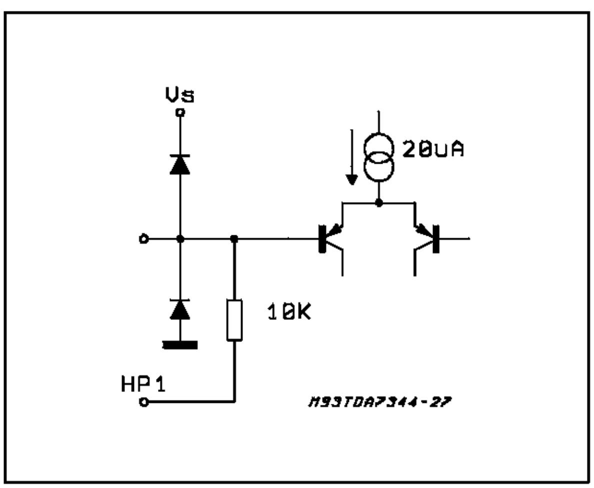
PIN: PS1



PIN: PS1A

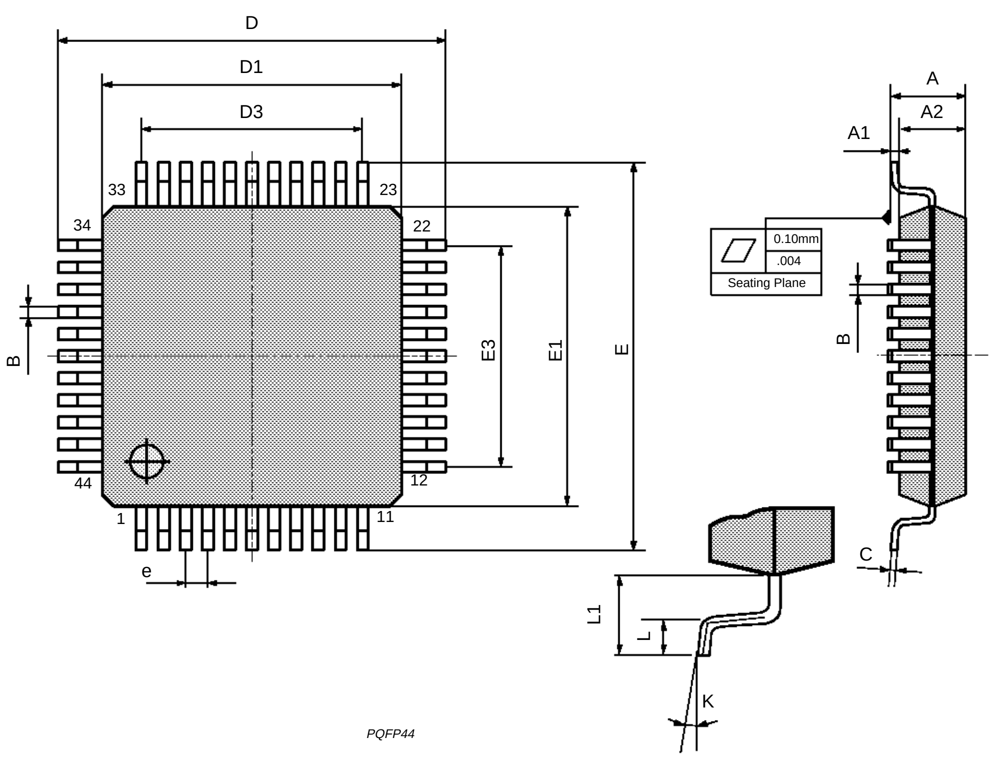


PIN: LP1



PQFP44 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.45			0.096
A1	0.25			0.010		
A2	1.95	2.00	2.10	0.077	0.079	0.083
B	0.30		0.45	0.012		0.018
c	0.13		0.23	0.005		0.009
D	12.95	13.20	13.45	0.51	0.52	0.53
D1	9.90	10.00	10.10	0.390	0.394	0.398
D3		8.00			0.315	
e		0.80			0.031	
E	12.95	13.20	13.45	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.394	0.398
E3		8.00			0.315	
L	0.65	0.80	0.95	0.026	0.031	0.037
L1		1.60			0.063	
K	0°(min.), 7°(max.)					



SDIP42 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			5.08			0.20
A1	0.51			0.020		
A2	3.05	3.81	4.57	0.120	0.150	0.180
B	0.36	0.46	0.56	0.0142	0.0181	0.0220
B1	0.76	1.02	1.14	0.030	0.040	0.045
c	0.23	0.25	0.38	0.0090	0.0098	0.0150
D	37.85	38.10	38.35	1.490	1.50	1.510
E	15.24		16.00	0.60		0.629
E1	12.70	13.72	14.48	0.50	0.540	0.570
e		1.778			0.070	
e1		15.24			0.60	
e2			18.54			0.730
e3			1.52			0.060
L	2.54	3.30	3.56	0.10	0.130	0.140